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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,824	08/01/2003	Xavier Montagne	003921.00143	1708

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EXAMINER	
TABLER, MATTHEW C	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/631,824	MONTAGNE ET AL.	
	Examiner	Art Unit	
	Matthew C. Tabler	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *16-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15, 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/24/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/631,824 filed on August 1st, 2003 by Montagna and Bedoiseau under assigne Mentor Graphics Corporation. Currently claims 1-38 are pending and claims 1-15 and 35-38 are elected.

Election/Restrictions

Applicant's election without traverse of claims 1-15 and 35-38 in the reply filed on July 25th, 2007 is acknowledged.

Claim Objections

Claims [2] and [4] are objected to because of the following informalities: In claim [2], line 2, "configuration bit look-up table" should be changed to "the configuration bit look-up table" so that it properly references the term in line 7 of claim [1]. In claim [4], line 2, "multiplexor" should be spelt "multiplexer". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims [1]-[15] and [35]-[38] are rejected under 35 U.S.C. 102(b) as being anticipated by Carter (US Patent 4,706,216) patented on November 10th, 1987.

In regard to claim [1], Carter shows an integrated circuit (Abstract), comprising a reconfigurable interconnect portion (Figure 8 – multiplexers 101-103; Column 8, line 64 – Column 9, line 39), a data processing portion coupled to the reconfigurable interconnect portion (logic elements 40-1 – 40-9 are shown in detail in Figure 7; data processing portion is the combinational logic 100), the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion (combinational logic block comprises registers that provide data to multiplexers; Column 9, lines 8-11), and a storage unit coupled to the data processing portion (Figure 7 – storage circuit 120; Column 9, lines 51-63), the storage unit including a configuration bit look-up table (Figure 8 shows a detailed schematic of the circuit shown in Figure 7; select logic 110 and 111 are look-up tables; Column 9, lines 21-24).

In regard to claim [2], Carter shows the integrated circuit wherein the integrated circuit includes a second reconfigurable interconnect portion (Figure 8 – multiplexers 104-106), and the configuration bit look-up table is configured to allow the data processing portion (combinational logic 120 receives signals from circuits 110 and 111) to extract a first set of configuration bits representing the bit pattern (several sets of configuration bits are received; see example in Column 8, line 64 – Column 9, line 3, i.e. A, B, C, and D) and to extract a second set of configuration bits representing a second bit pattern to load a second configuration of the second reconfigurable interconnect portion (i.e. A, B, C, and Q), wherein the second set is a subset of the first set (Column 10, lines 22-30).

In regard to claim [3], Carter shows the integrated circuit wherein the reconfigurable interconnect portion comprises a switching matrix (configurable logic element apart of larger switching matrix circuit shown in Figure 4A).

In regard to claim [4], Carter shows the integrated circuit wherein reconfigurable interconnect portion comprises a multiplexer (multiplexers 101-106 shown in Figure 8).

In regard to claim [5], Carter shows the integrated circuit wherein the switching matrix includes a control signal input configured to select between two inputs to connect to an output (Figure 7 shows output circuit as 'select logic 140' which selects between two inputs to connect to an output; Column 8, lines 60-63).

In regard to claim [6], Carter shows the integrated circuit wherein the reconfigurable interconnect portion comprises a pair of transistors (reconfigurable interconnect multiplexers comprise several pairs of transistors).

In regard to claim [7], Carter shows the integrated circuit wherein the reconfigurable interconnect portion comprises a plurality of memory elements (Column 8, lines 51-60), each memory element connected to at least one switch of the reconfigurable interconnect portion (see Figure 8).

In regard to claim [8], Carter shows the integrated circuit wherein the bit pattern is derived from the configuration bit look-up table (Column 9, lines 21-24).

In regard to claim [9], Carter shows the integrated circuit wherein the configuration bit look-up table comprises a plurality of rows of configuration bits (RAM 108 has selectable locations; Column 9, lines 21-24).

In regard to claim [10], Carter shows the integrated circuit wherein the storage unit is coupled to the data processing portion by a plurality of address lines for accessing the rows of configuration bits stored within the storage unit (RAM 108 has selectable locations; Column 9, lines 21-24).

In regard to claim [11], Carter shows the integrated circuit wherein the storage unit further comprises programming instructions configured for accessing the configuration bit look-up table (each of the configurable switches 101-106 is configured with control bits from a programming register; Column 9, lines 9-11), wherein the programming instructions are further configured for extracting a subset of configuration bits from the configuration bit look-up table (Column 9, lines 21-24).

In regard to claim [12], Carter shows the integrated circuit wherein the data processing portion (Figure 8 – 100) is configured to map a first input (circuit 112 receives inputs from 110 and 111) of the reconfigurable interconnect portion to a first output of the reconfigurable interconnect portion in response to a first command (command from signal B may pass input from circuit 110; Column 9, lines 21-28).

In regard to claim [13], Carter shows the integrated circuit wherein the data processing portion (Figure 8 – 100) is configured to map a second input (circuit 112 receives inputs from 110 and 111) of the reconfigurable interconnect portion to a second output of the reconfigurable interconnect portion in response to the first command (command from signal B may pass input from circuit 111; Column 9, lines 21-28).

In regard to claim [14], Carter shows the integrated circuit wherein the data processing portion (Figure 8 – 100) is configured to map a second input (second input to 114 from circuit

111) of the reconfigurable interconnect portion to a second output (F1) of the reconfigurable interconnect portion in response to a second command (command on line 115; Column 9, lines 28-32).

In regard to claim [15], Carter shows the integrated circuit further comprising a second reconfigurable interconnect portion (Figure 8 – circuits 104-106), and wherein the data processing portion (Figure 8 – 100) is configured to map a first input (first input to 114 from circuit 111) of the second reconfigurable interconnect portion to a first output (F1) of the second reconfigurable interconnect portion in response to a second command (command on line 115; Column 9, lines 28-32).

In regard to claim [35], Carter shows an integrated circuit comprising a reconfigurable interconnect portion (Figure 7 – combinational logic 100) and a storage unit (storage circuit 120) coupled to the reconfigurable interconnect portion (see Figure 7), wherein the storage unit stores a look-up table for use in configuring the reconfigurable interconnect portion (Column 9, lines 21-24).

In regard to claim [36], Carter shows an integrated circuit (Figure 8), comprising a reconfigurable interconnect portion (multiplexers 101-103), a data processing portion (combinational logic 100) coupled to the reconfigurable interconnect portion (see Figure 8), the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion (combinational logic block comprises registers that provide data to multiplexers; Column 9, lines 8-11), and a storage unit (select logic 140) coupled to the data processing portion (see Figure 8), the storage unit including a look-up table, wherein the look-up table (Column 9, lines 21-24) is configured to

allow the data processing portion (combinational logic 120 receives signals from circuits 110 and 111) to extract a first set of bits representing the bit pattern (several sets of configuration bits are received; see example in Column 8, line 64 – Column 9, line 3, i.e. A, B, C, and D) and to extract a second set of bits representing a second bit pattern (i.e. A, B, C, and Q) to load a second configuration of a second reconfigurable interconnect portion (multiplexers 104-106), wherein the second set is a subset of the first set (Column 10, lines 22-30).

In regard to claim [37], Carter shows a method of configuring a reconfigurable interconnect portion, comprising steps of determining configuration bits to configure the reconfigurable interconnect portion (multiplexers 101-103), accessing a configuration bit-look up table (Column 9, lines 21-24), extracting a set of configuration bits representing the bit pattern from the configuration bit look-up table (outputs the bits stored in look-up memory), and providing the set of configuration bits representing the requested bit pattern (see Figure 8).

In regard to claim [38], Carter shows a method of configuring a reconfigurable interconnect portion of a circuit (Figure 8), comprising steps of receiving a set of configuration bits representing the requested bit pattern (several sets of configuration bits are received; see example in Column 8, line 64 – Column 9, line 3, i.e. A, B, C, and D), and configuring a reconfigurable interconnect portion based on the received configuration bits (Column 8, line 64 – Column 9, line 61), wherein the configuration bits are derived from a configuration bit look-up table (circuits 110 and 111).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Tabler whose telephone number is (571) 270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MCT
August 27, 2007

Rexford Barnie

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER

08/27/07